Office of the Registrar FORM 40 REV. 2/99

PURDUE UNIVERSITY REQUEST FOR ADDITION, DELETION, OR REVISION OF A COURSE

SCHOOL DOCUMENT NO. EFD 8-01

GRADUATE COUNCIL DOCUMENT NO. 02-9b

EPARTMENT School of Electrical and Computer Engineering

DATE SUBMITTED 12/7/2001

DATE EFFECTIVE Fall 2002

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INSTRUCTIONS: Please check the items below which describe the purpose of this request. PURPOSE											
1. Deletion of a course New course with support Add existing course of Change in course nurrence Change of Change o	Chang Chang Chang Chang Chang	Change in semesters offered Change in course credit/type Change in course attributes Change in instructional hours Change in prerequisites Change in description of course content Transfer of course from one dept. to another									
EXISTING:	PROPOSED:					SEMESTERS OFFERED					
Subject Abbreviation EE Subject Abbreviation EE Course Number 670 Course Number 670 Proposed Title Modeling and Optimization of High-Performance Interconnects					Check Sumr	All That Apply. ner Fall Ag Winter Spring					
Variable Title Yes No V											
Abbreviated Title Abbreviated title will be entered by the Office of the Registrar if omitted. (22 CHARACTERS ONLY)											
CROSS LISTED COURSES THE PROPERTY OF THE PROP	Min (Ch Max	edit: Cr. Hrs Credit Range: imum Cr. Hrs eck One) To kimum Cr. Hrs,	Or No Separation	1. F 2. F 3. A 4. E 5. S	Pass/Not Pass Onl Repeatable for Credi Available for Credi Designator Require Special Fees Approval Required Dep	dit t by Examination ad					
Type Hours Ty Primary 3 At Secondary In Laboratory CI		Hours		Class Hours	<u>FTE</u> данталь торорь «порагойнариля «порагодором»	CAMPUS(ES) INVOLVED Calumet Fort Wayne Indianapolis North Central West Lafayette Off Campus					
COURSE DESCRIPTION (PREREQUISITES INCLUDED): Prerequisites: EE 559 for equivalent, and EE 608 for equivalent), or consent of instructor. RLC extraction of VLSI interconnects. Modeling of interconnects as RLC trees or networks. Elmore delay model. Reduced-order modeling: moment matching, Padé approximation, and Krylov-subspace methods. Device modeling with consideration of resistive shielding in the interconnection load. Delay calculation with consideration of devices and interconnects. Repeater insertion and planning at floorplanning. Timing-driven placement: zero-slack algorithm for delay budgeting, net-based placement, path-based placement. High-performance clock synthesis: zero-skew routing, bounded-skew routing, useful-skew routing. Term projects investigating interconnect-related issues will be assigned. Professor Koh. and are											
Calumet Undergrad Curriculum Committee	Date Calu	ımet Department Head		Date	Calumet School [Dean Da					
Fort Wayne Department Head	Date Fort	Wayne School Dean		Date	Fort Wayne Char Appr. for Fac C.D.Sutton,C	ilty #958					
Indianapolis Department Head	Date India	anapolis School Dean		Date	Undergrad Curric						
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North Central Department Head	Date Nort	h Central Vice Chancello	nr.	Date		y Graduate Council					
st Lafayette Department Head	>	t Lafayette School Dean	agus 9	Taling Date	Tarily Graduate Connci	A. Seistolislo					
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Graduate Area Committee Convener	Date Grad	duate Dean		Date	West Lafayette R	egistrar Da					

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